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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,325	10/21/2003	Lee Doyle Whetsel	TI-14124D.5	1606
23494	7590	04/29/2005	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			BRITT, CYNTHIA H	
			ART UNIT	PAPER NUMBER
			2133	

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,325	WHETSEL, LEE DOYLE	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 25-56 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 25-33 and 35-40 is/are allowed.
- 6) ☒ Claim(s) 41-43, 45-49, 52, 53, 55 and 56 is/are rejected.
- 7) ☒ Claim(s) 34, 44, 49-51 and 54 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>10/21/03</u> . | 6) <input type="checkbox"/> Other: _____ |

Handwritten mark

DETAILED ACTION

Claims 25-56 are presented for examination.

Claims 1-24 have been cancelled.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on October 21, 2003 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

The examiner would like to point out that although applicant has discussed numerous US patents, none of the discussed US patents are listed on the form 1449. The examiner requests applicant to submit another form 1449 listing all US references discussed in applicant's remarks in the Preliminary Amendment A pages 22-26.

Drawings

The drawings were received on October 21, 2003. These drawings are acceptable.

Claim Objections

Claims 34 and 49 are objected to because of the following informalities: "...and scanning the stored data out of the data sample register on a scan path that is coupled to the data sample register and that extends to a scan data output on the integrated circuit", is unclear. Appropriate correction is required.

Allowable Subject Matter

Claims 25-40 are allowable over the prior arts of record. (Objection to claim 34 must be addressed)

Independent claim 25 requires: scanning a first signal into a serial scan path in response to a scan clock signal and a mode signal; storing the first signal, which indicates desired protocol; comparing operating signals of functional circuits to compare signals; generating or detecting an event signal indicating a match; and performing circuit operation on the integrated circuit using the desired protocol. In the disclosed combination, the prior arts fail to teach the above.

Claims 44, 50, 51, 54 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Preliminary Amendment

In the "Remarks" section of the preliminary amendment, page 21 paragraph 6, applicant states "Independent claims 25 and 41 distinguish over the art by requiring: ...comparing operating signals of functional circuits to compare signals; ... indicating a match; and performing circuit operation on the integrated circuit using the desired protocol." Although claim 25 does recite these limitations, claim 41 fails to recite comparing or indicating a match.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Binoeder et al. U.S. Patent No. 4,620,302 in view of "Structured Computer Organization" by Andrew Tanenbaum 1984.

As per claim 41, Binoeder et al. substantially teach the claimed method of operating a circuit system in which a test being preformed using a multi-protocol system that uses a protocol which is stored in a register (column 19 lines 27-40, figure 7), and a selection of certain events are utilized for diagnostic purposes using functional and software test programs (column 3 lines 1-4). A Flag RAM (random access memory) is used by the micro-controller to remember events pertaining to the line protocol and error handling procedures (Column 21 lines 42-46). Although Binoeder et al. teach this

process using a software method, in an analogous art, Tanenbaum teaches that any operation performed by software can also be directly built into hardware and any instruction executed by the hardware can also be simulated in software. Therefore, hardware and software are logically equivalent. (Page 11 lines 10-15) Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used either a hardware or software method of operation for the circuit. This would have been obvious as suggested by Tanenbaum (page 11 lines 15-19) since it would be the choice of the designer as there are no hard and fast rules governing which should be used in any situation.

As per claims 42, 43, 45, and 46 Binoeder et al. teach that each byte of data received is loaded into descending bytes of the receive register. The byte to be loaded is addressed by the byte counter and when a complete word has been stored in the receiver register, then the micro-controller does a map entry to the subroutine indicated by the "word-type" in the receive register. This micro-code subroutine will either move the receive register contents to a designated location in the tester system or else perform a direct command (column 19 lines 41-53, column 8 line 49 through column 9 line 7).

As per claims 47-49, Binoeder et al. teach that the input/output register is an eight-bit register, which can be parallel loaded from the OUT MUX. It can also be serial loaded from the CRC checker generator in order to send generated CRC code at the end of a message. The I/O register can be serially shifted out into the CRC checker generator for checking or generating CRC codes. The I/O register is also used in

conjunction with the I/O comparator for character recognition on the incoming data from the driver. This is done to verify the line protocol. The input/output comparator is an eight-bit comparator circuit that compares the contents of the I/O register to a value supplied by the micro-controller over the maintenance data bus MNTD. The result of the comparison was sent back to the micro-controller as a test condition for subsequent decision-making. The main use is in the execution of the data communications protocol (column 21 lines 24-41).

As per claims 52 and 53, Binoeder et al. teach the code processor controls the "event" logic in the module, which counts events as requested by the technician. The event logic includes a clock counter, a synchronization counter, a programmable event counter, an execution counter and a T counter which are described in connection with the event module (column 9 lines 57-63, also column 26 lines 31-64).

As per claims 55 and 56, Binoeder et al. teach that in conjunction with the utility register, virtually any pattern can be generated for a particular application. In FIG. 11D the shift register can be loaded from the TO bus. Thus, the output of any of the other registers of the buffer memory or the D bus can be placed into the shift register of FIG. 11D. The output of the 20-bit shift register then provides the input to the pattern memory and also the Fm bus. When the shift register is in the shift mode, it moves data from the least significant bit to the most significant bit. The pattern memory has an output which is a shift data line which is conditioned by the data shift from the shift register, and from the 20-bit shift register and the two select lines, which come from the card ELSCI4 of FIG. 11A. (Figures 11A-D and column 32 lines 27-50)


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Cynthia Britt
Examiner
Art Unit 2133


GUY LAMARRE
PRIMARY EXAMINER